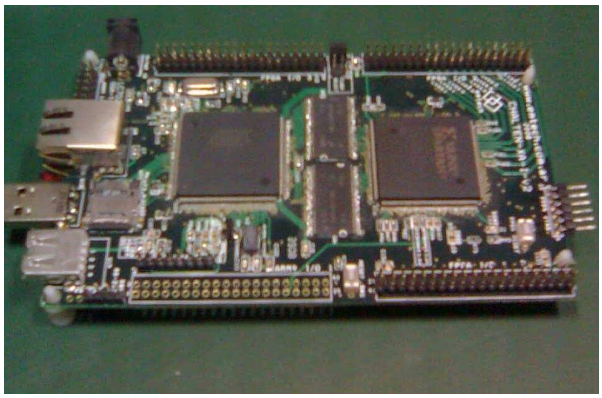
CHALTEN XA 1

Descripción de la placa.



Autor	Nombre del autor
Versión	0.1
Ultima revisión	Fecha de la última revisión

Contenido

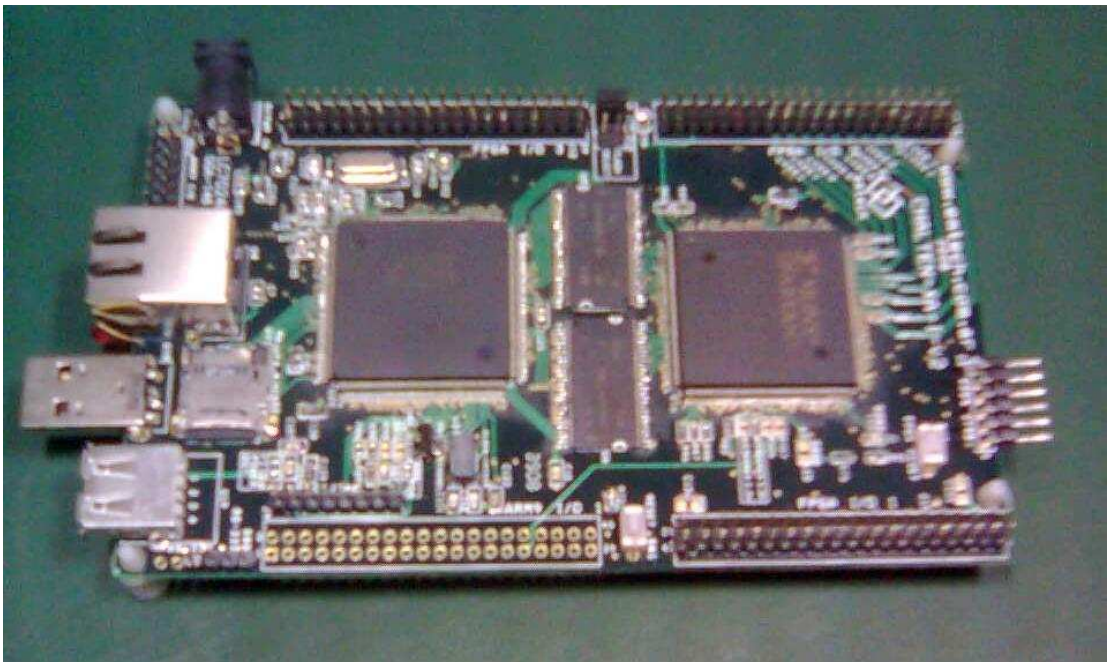
Revisiones

Fecha	Versión	Modificaciones
Enero 5, 2008	0.1	• Versión original
Junio 30, 2008	0.2	• Modifica 1 • Modifica 2

1 Introducción

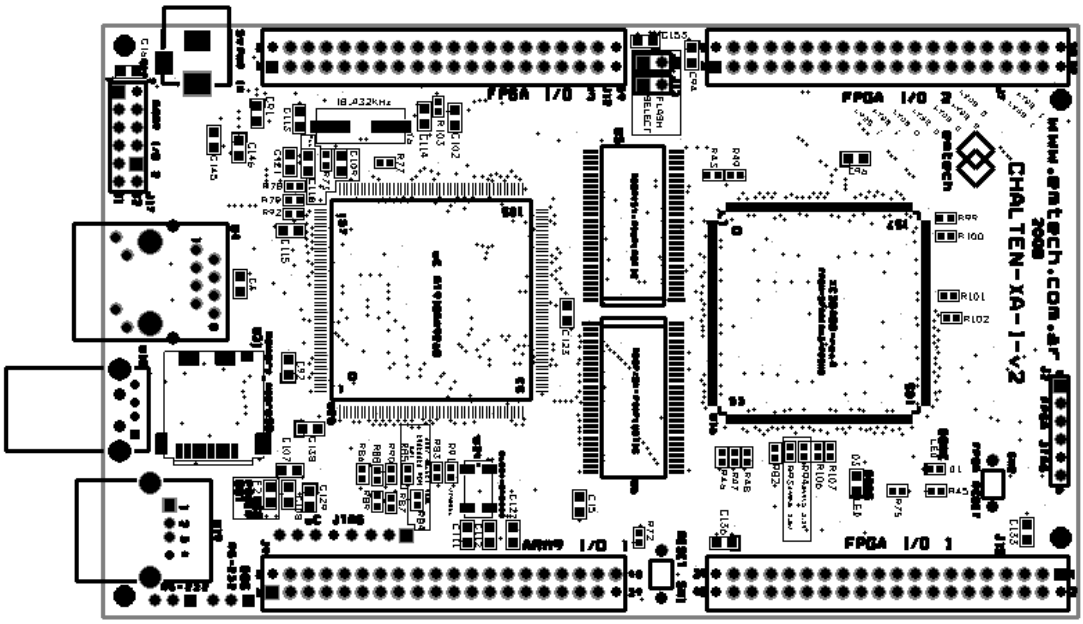
En este documento se describe las características de la placa, componentes existentes e interfaces entre ellos y el usuario.
Con este documento podemos analizar el alcance y posibilidades de desarrollo utilizando a CHALTEN.

Esta placa fue creada para realizar proyectos que requieran gran poder de procesamiento, altas velocidades de transferencia de datos y numerosas entradas-salidas (I/O) para placas “hijas” con las cuales podemos ampliar la capacidad inicial de la placa agregando los componentes deseados.



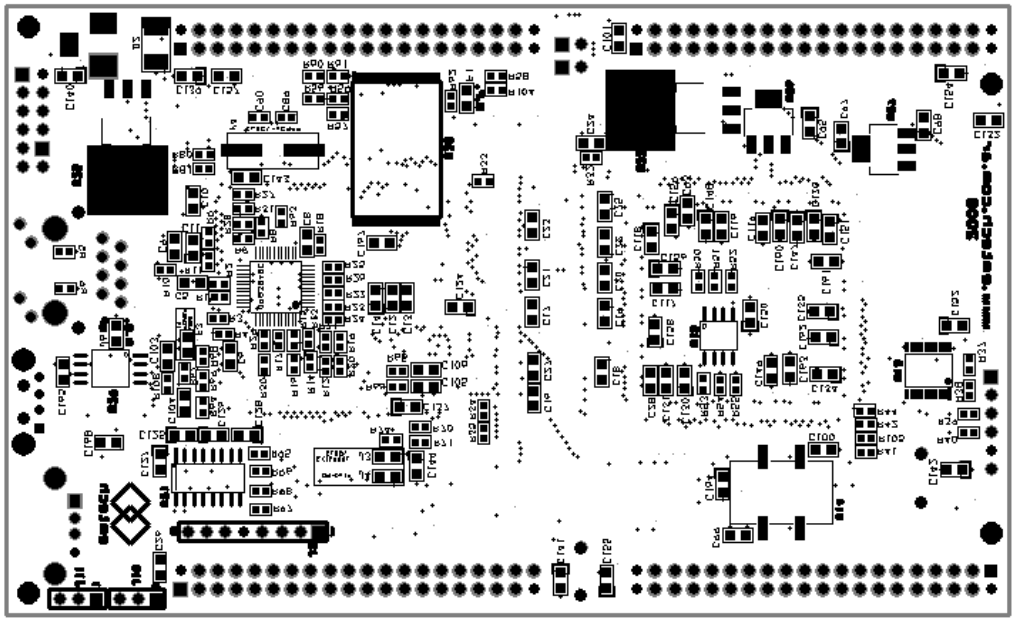
2 Descripción de la placa

2.1 Vista superior



1-Vista superior

2.2 Vista Inferior



2-Vista inferior

2.3 Componentes en la placa

- **FPGA Spartan-3 XC3S400**
  Serial **EEPROM** 24LC128
  PROGRAM MEMORY **XCF02S**
  JTAG/ICE debug interface
  three expansion connectors 3x30 I/Os

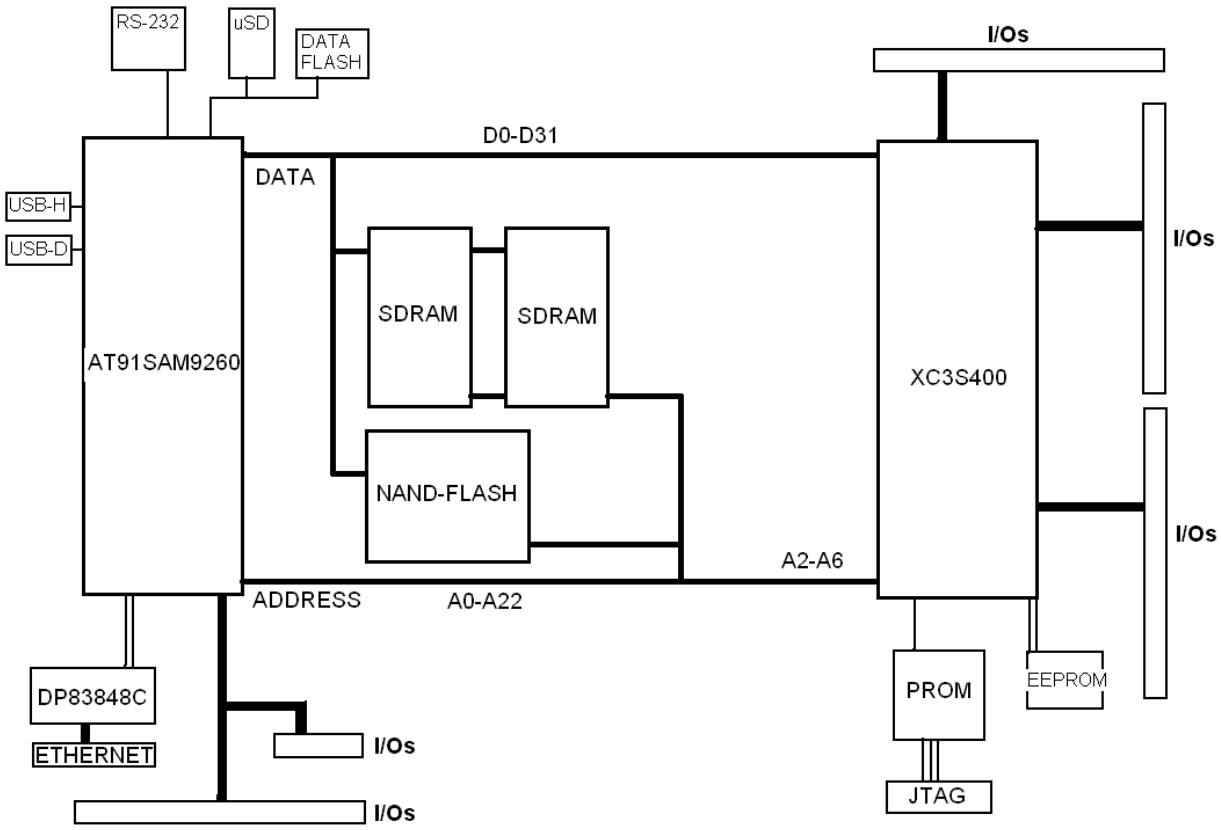
- **MICROPROCESADOR ATMEL AT91SAM9260**
  64 Mbytes of **SDRAM** memory
  1 Gbytes of **NANDFlash** memory
  one Atmel serial **DataFlash**
  one **USB device** port interface
  one **USB Host** port interfaces
  one DBGU **serial communication** port
  handshake control
  JTAG/ICE debug interface
  one PHY **Ethernet** 10/100-base TX with three status LEDs
  one reset push button
  one **DataFlash** and **uSD** card slot
  two expansion connectors (1x36 I/Os + 1x10 I/Os)

- **Power regulador** 5VDC to 3.3v, 2.5v and 1.8v.

2.4 Requerimientos

AC/DC power adapter 5VDC 2Amp 2.1mm x 5.5mm

2.5 Conexiones en la placa



3- esquema de conexión

3 Microprocesador AT91SAM9260

3.1 AT91SAM9260

The AT91SAM9260 is the first member of a pin-compatible ARM9-based microcontroller family that shares the same programming model as ARM7-based controllers, allowing direct migration between controllers based on different ARM cores. It supports deterministic, real-time operation, offers supervisory functions, and has third-party support comparable to that for 8-bit microcontrollers.

The AT91SAM9260 is based on the ARM926EJ-S processor, with 8K byte instruction and 8K byte data cache memories. It operates at 210 MIPS with a 190 MHz clock. It features 8K bytes of SRAM and 32K bytes of ROM with single cycle access at maximum processor or bus speed, together with an external bus interface with controllers for SDRAM and static memories including NAND Flash and CompactFlash. Its extensive peripheral set includes USB Full Speed Host and Device interfaces, a 10/100 Base T Ethernet MAC, Image Sensor Interface, Multimedia Card Interface (MCI), Synchronous Serial Controllers (SSC), USARTs, Master/Slave Serial Peripheral Interfaces (SPI), a three-channel 16-bit Timer Counter (TC), a Two Wire Interface (TWI) and four-channel 10-bit ADC. Three 32-bit Parallel I/O Controllers multiplex the pins to/from these peripherals in order to reduce the device pin count, and peripheral DMA channels maximize the data throughput between these interfaces and the on- and off-chip memories.

The AT91SAM9260 has a fully featured system controller for efficient system management, including a reset controller, shutdown controller, clock management, advanced interrupt controller (AIC), debug unit (DBGU), periodic interval timer, watchdog timer and real-time timer. It is available in a 217-ball LFBGA RoHS-compliant package and in a 208-pin Green QFP package.

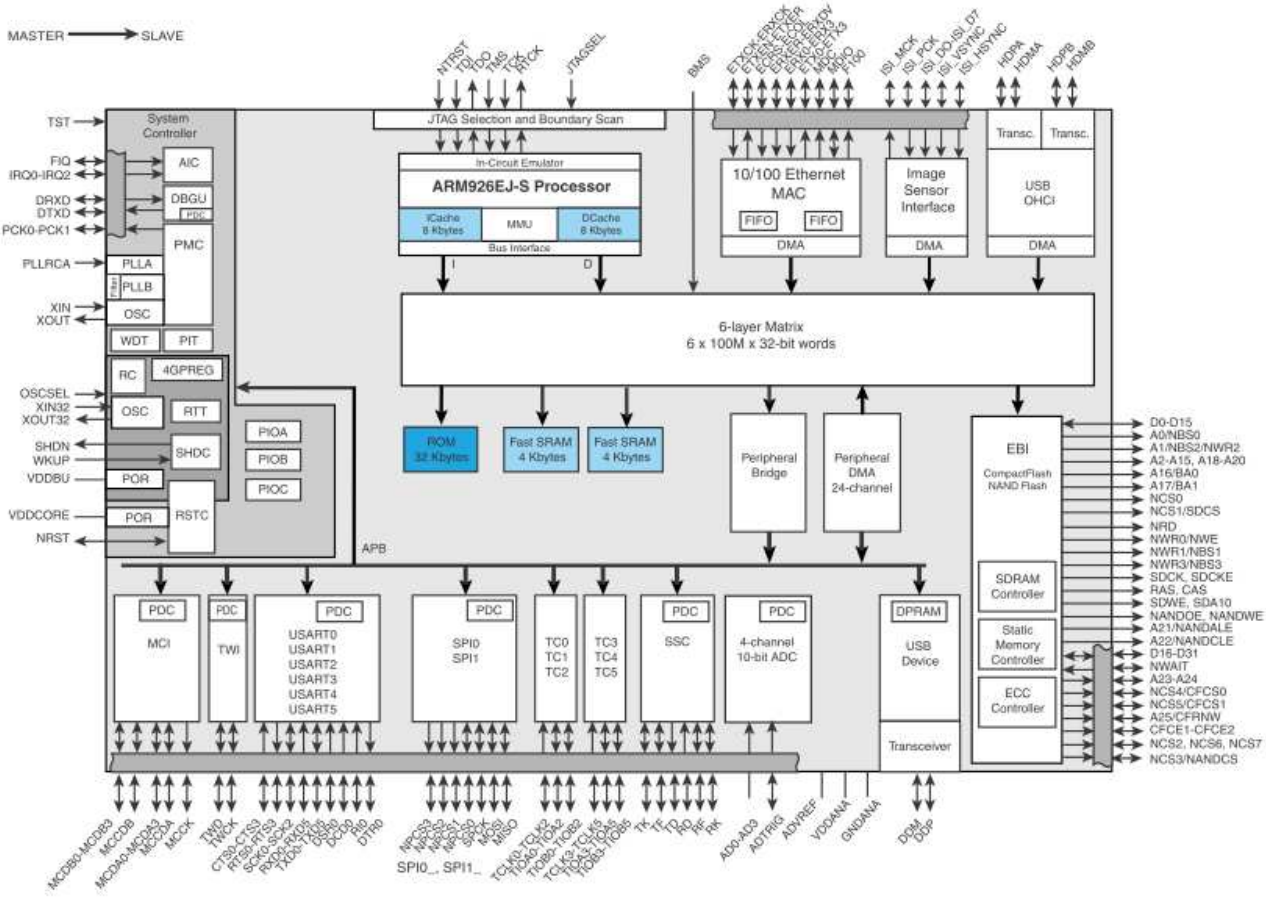
3.2 Especificaciones del microprocesador

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, ARM Jazelle® Technology for Java® Acceleration
  - 8-KByte Data Cache, 8-KByte Instruction Cache, Write Buffer
  - 200 MIPS at 180 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
- Additional Embedded Memories
  - One 32-KByte Internal ROM, Single-cycle Access At Maximum Matrix Speed
  - Two 4-KByte Internal SRAM, Single-cycle Access At Maximum Matrix Speed
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, ECC-enabled NANDFlash and CompactFlash®
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM

- USB 2.0 Full Speed (12 Mbits per second) Host Single Port in the 208-lead PQFP
  - – Single or Dual On-chip Transceivers
  - – Integrated FIFOs and Dedicated DMA Channels
- Ethernet MAC 10/100 Base T
  - – Media Independant Interface or Reduced Media Independant Interface
  - – 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Image Sensor Interface
  - – ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - – 12-bit Data Interface for Support of High Sensibility Sensors
  - – SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- Bus Matrix
  - – Six 32-bit-layer Matrix
  - – Boot Mode Select Option, Remap Command
- Fully-featured System Controller, including
  - – Reset Controller, Shutdown Controller
  - – Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - – Clock Generator and Power Management Controller
  - – Advanced Interrupt Controller and Debug Unit
  - – Periodic Interval Timer, Watchdog Timer and Real-time Timer
- Reset Controller (RSTC)
  - – Based on a Power-on Reset Cell, Reset Source Identification and Reset Output Control
- Clock Generator (CKGR)
  - – Selectable 32768Hz Low-power Oscillator or Internal Low Power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - – 3 to 20 MHz On-chip Oscillator, One up to 240 MHz PLL and One up to 130 MHz PLL
- Power Management Controller (PMC)
  - – Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - – Two Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - – Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - – Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - – 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - – 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - – Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-time Timer (RTT)

  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- One 4-channel 10-bit Analog-to-Digital Converter
- Three 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC)
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
  - High-current Drive I/O Lines, Up to 16 mA Each
- Peripheral DMA Controller Channels (PDC)
- One Two-slot MultiMedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
  - One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation,
    Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Signal Control on USART0
- Two 2-wire UARTs
- Two Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - Synchronous Communications
- Two Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
  - High-Drive Capability on Ouputs TIOA0, TIOA1, TIOA2
- One Two-wire Interface (TWI)
  - Master, Multi-master and Slave Mode Operation
  - General Call Supported in Slave Mode
  - Connection to PDC Channel To Optimize Data Transfers in Master Mode Only
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.65V to 1.95V for VDDBU, VDDCORE, VDDOSC and VDDPLL
  - 3.0V to 3.6V for VDDIOP0, VDDIOP1 (Peripheral I/Os) and VDDANA (Analog to Digital Converter)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in a 208-lead PQFP

3.3 Diagrama en bloque del microprocesador



4-Diagrama del uP

4 **FPGA Spartan-3** XC3S400

4.1 Spartan-3

The Spartan™-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The eight-member family offers densities ranging from 50,000 to five million system gates, as shown in Tabla 1.
The Spartan-3 family builds on the success of the earlier Spartan-IIE family by increasing the amount of logia resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. Numerous enhancements derive from the Virtex™-II platform technology. These Spartan-3 enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.
Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home network- ing, display/projection and digital television equipment.
The Spartan-3 family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

4.2 Atributos de XC3S400

Device	System Gates	Equivalent Logic Cells[1]	CLB Array (One CLB = Four Slices)			Distributed RAM Bits (K=1024)	Block RAM Bits (K=1024)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50[2]	50K	1,728	16	12	192	12K	72K	4	2	124	56
XC3S200[2]	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400[2]	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000[2]	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000	4M	62,208	96	72	6,912	432K	1,728K	96	4	712	312
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	784	344

Tabla 1

4.3 Especificaciones de Spartan-3

- Low-cost, high-performance logic solution for high-volume, consumer-oriented applications
  - Densities up to 74,880 logic cells
- SelectIO™ signaling
  - Up to 784 I/O pins
  - 622 Mb/s data transfer rate per I/O

  - 18 single-ended signal standards
  - 8 differential I/O standards including LVDS, RSDS
  - Termination by Digitally Controlled Impedance
  - Signal swing ranging from 1.14V to 3.45V
  - Double Data Rate (DDR) support
  - DDR, DDR2 SDRAM support up to 333 Mbps
- Logic resources
  - Abundant logic cells with shift register capability
  - Wide, fast multiplexers
  - Fast look-ahead carry logic
  - Dedicated 18 x 18 multipliers
  - JTAG logic compatible with IEEE 1149.1/1532
- SelectRAM™ hierarchical memory
  - Up to 1,872 Kbits of total block RAM
  - Up to 520 Kbits of total distributed RAM
- Digital Clock Manager (up to four DCMs)
  - Clock skew elimination
  - Frequency synthesis
  - High resolution phase shifting
- Eight global clock lines and abundant routing
- Fully supported by Xilinx ISE™ and WebPACK™ development systems
- MicroBlaze™ and PicoBlaze™ processor, PCI®, PCI Express® PIPE Endpoint, and other IP cores
- Pb-free packaging options
- Automotive Spartan-3 XA Family variant

5 Software utilizado

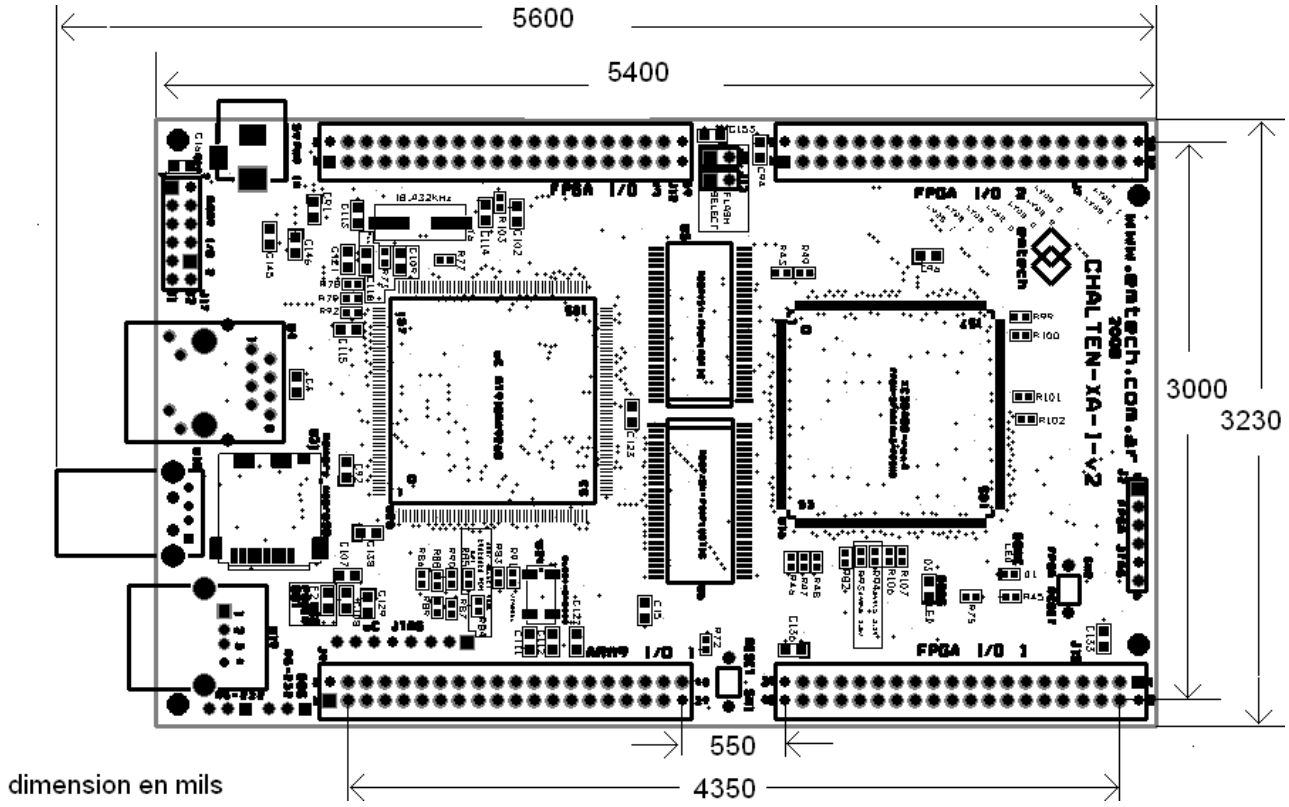
El procesador es utilizado en la placa como una unidad de procesamiento general, es decir para diferentes tareas de control del sistema. Además, al disponer de un sistema operativo, brinda soporte para múltiples interfaces de comunicación estándard con poco esfuerzo. Esto permite tener una gran flexibilidad en el modo de uso de la placa en distitos tipos de sistemas embebidos. En caso de requerirse procesamiento mas intensivo (DSP) o interfaces específicas, etc., esas tareas serán realizadas por la fpga.
Sobre el procesador ARM9 puede ejecutarse uno de varios sistemas operativos disponibles:

- Linux
- WinCE
- µC/OS-II - Real-Time Kernel
- FreeRTOS
- etcétera

El sistema operativo elegido para ser utilizado en la placa es linux, debido a que este provee soporte para todas las interfaces disponibles (usb host y device, ethernet, SD Card, etc.). Además, al ser un sistema operativo de código abierto es posible realizar extensiones para dar soporte a las carácterísticas particulares de la placa, en especial la interfaz con la fpga y con el conector de expansión del micro. Esto se consigue por medio de drivers que se compilan como módulos del kernel. Estos módulos se compilan en forma separada del kernel, lo que permite realizar drivers a medida para distintas aplicaciones sin tener que recompilar el kernel.
El filesystem que se programa en la placa, es decir el conjunto de aplicaciones que el sistema puede correr, se cross-compila en una PC. Se ha utilizado el sistema buildroot, que permite seleccionar los paquetes de software que se desea instalar. Luego estos paquetes se compilan generando una imagen del filesystem en formato jffs2, que es el necesario para descargar en la memoria nand flash de la placa.
Algunas de las herramientas que han sido probadas son:

- Acceso a memorias de almacenamiento masivo (pendrive, SD Card). Estas memorias se montan en el filesystem de linux y pueden accederse para realizar escrituras y lecturas.
- Ethernet: mediante IP estática o utilizando DHCP puede conectarse a una red local y de esta manera acceder desde la placa hacia el exterior (internet) o desde una PC hacia la placa, por ejemplo mediante SSH. De esta manera se puede controlar el funcionamiento del sistema en forma remota. También se pueden realizar transferencias de archivos desde y hacia la placa.
- Mediante la interfaz serie de la placa se puede acceder a la línea de comandos del bootloader, utilizando por ejemplo el HiperTerminal de windows, y de esta manera programar un nuevo kernel, cargar un nuevo filesystem en la memoria flash, montar el filesystem desde un pendrive, entre otras. Todas estas alternativas pueden utilizarse para simplificar la depuración de aplicaciones, actualizar versiones de software, programación en campo de placas, etc.

6 Dimensiones


5600
5400
3000
3230
550
4350
dimension en mils
CHALTEN-XA-1-V2
FPGA I/O 3
FPGA I/O 2
FPGA I/O 1
ARM9 I/O 1