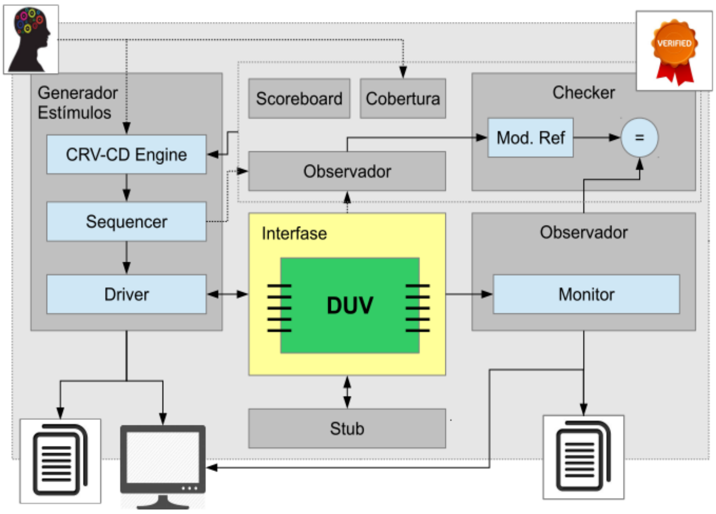
SoC Advanced Verification Environment Development



Technical characteristics

- Object Oriented Programming based Testbench.
- Scalable
- Maintainable
- Reusable.
- Advanced Test Design & Coverage Analysis.

Technologies & Tools

- System Verilog & UVM.
- VHDL & Verilog.
- Constrained Random Verification (CRV).
- System Verilog Assertions (SVA)
- Code & Functional Coverage.
- Formal Verification.
- C/C++ & Matlab.
- Direct Programming Interface (DPI)
- FPGA based Emulation
- Debugging Tools.
- Scripting languages (Tcl, Python).

Project Description

This project consisted in the Verification of the System On Chip (SoC) designed to be the main controller of a Critical System and implemented into a multimillion gate FPGA. The SoC incorporates a general purpose processor, several application specific cores and controllers; all connected with a multi-master AXI bus and fault detection & recovery resources. It also handles several dedicated interfaces with stringent timing constraints, as well as standard IO for DRAM, SRAM, Ethernet, USB and I2C interfaces.

Emtech lead the overall verification process, from test plan definition, to testbench implementation, DUV simulation and bug tracking. The verification environment was developed in System Verilog as a new instance of our continuously improved framework. The UVM base library was employed for the testbench architecture and in-house developed verification IPs (Agents) where integrated and reused. SV classes were extensively used to manage a complex Loosely Timed reference model that involves an instruction level simulator for the CPU and allows emulating all the high level transactions derived from ambitious functional coverage requirements.

Experience & Skills

- “State of the art” functional verification methodologies.
- OOP Verification Environment development & Verification IP integration.
- Functional Coverage Space modeling and an0alysis
- Formal Verification.
- Event Driven Simulation & Debugging.
- Digital Electronics.
- Standard SoC components & IO: ARM Cortex, AMBA AHB-AXI, Ethernet, USB and I2C.
- ASIC & FPGA design & verification flows: Logic Synthesis, Static Timing Analysis, Clock Domain Crossing, Power Management, and Place & Route.
- System Bring Up & Silicon Validation – Lab measurements.
- Verification planning and management.

Industry and Applications

- Technology Developers.
- Consumer Electronics.
- Verification IP.
- Microelectronics.
- Computer Hardware.
- Critical Systems.

Viamonte 685 - 8000. Bahía Blanca. Buenos Aires. Argentina. ☎ +542914532918.
Gallardo 855 – 8400. Bariloche - Río Negro. Argentina. ☎ +542944458554.
www.emtech.com.ar ✉ info@emtech.com.ar